In the Claims:

1. (Currently Amended) An automatic machine-implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

automatically enlarging a spacing between neighboring features of a path of the layout by a predetermined incremental spacing provided that the length of the path does not then exceed a predetermined dimensional constraint and provided that connectivity is maintained between the neighboring features and any features of the layout to which the neighboring features are connected; and

repeating said enlarging for at least one other spacing of the layout.

2. (Currently Amended) The method of ~~A method of de-compacting a layout as claimed in~~ claim 1 wherein said enlarging is repeated until all enlargeable spacings of said layout are enlarged.

3. (Currently Amended) The method of ~~A method of de-compacting a layout as claimed in~~ claim 2 wherein said spacings are enlarged in order from a smallest said spacing in said layout.

4. (Currently Amended) The method of ~~A method of de-compacting a layout as claimed in~~ claim 1 wherein said predetermined dimensional constraint is a critical path length (C) of said layout in a first direction of said layout.

5. (Currently Amended) The method of ~~A method of de-compacting a layout as claimed in~~ claim 1 wherein said predetermined dimensional constraint represents a dimension of an area available for said layout in a first direction.

6. (Currently Amended) The method of ~~A method of de-compacting a layout as claimed in~~ claim 2 wherein said predetermined dimensional constraint limits the length of said path in a first direction of the layout, wherein said neighboring features include a first feature and a second feature neighboring said first feature of said spacing, wherein said path includes a first neighbor spacing between said first feature and a third feature neighboring said first feature, and when said path includes a fourth feature neighboring said second feature, said path further includes a second neighbor spacing between said second feature and said fourth feature,

wherein said spacing is enlarged only when said spacing is smaller than the larger of said first neighbor spacing and said second neighbor spacing by a predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said spacing is enlarged only when said spacing is smaller than said first neighbor spacing by said predetermined amount.

7. (Canceled)

8. (Currently Amended) The method of ~~A method of de-compacting a layout as claimed in~~ claim [[7]] 6 wherein when said spacing of said path is enlarged, the larger of said first neighbor spacing and said second neighbor spacing is reduced by said predetermined amount when said path includes said fourth feature, and when said path does not include said fourth feature, said first neighbor spacing is reduced by said predetermined amount.

9. (Currently Amended) The method of ~~A method as claimed in~~ claim 8 wherein each said spacing is enlarged as many times as enlargeable.

10. (Currently Amended) A method of de-compacting ~~decompacting~~ a layout of a portion of an integrated circuit, comprising:

a) providing a predetermined dimensional constraint for said layout in a first direction of said layout;

b) automatically enlarging a spacing between first and second features of a path of said layout by a predetermined amount, provided that the length of said path does not then exceed said predetermined dimensional constraint and provided that connectivity is maintained between said first and second features and any features of the layout to which said first and second features are connected, when said spacing is smaller by said predetermined amount than the larger of a first neighbor spacing between said first feature and a third feature of said path neighboring said first feature, and a second neighbor spacing between said second feature and a fourth feature of said path neighboring said second feature; and

c) repeating said step b) in order from a smallest said spacing enlargeable by said step b) until all spacings enlargeable by said step b) are enlarged as many times as enlargeable.

11.-30. (Canceled)

31. (New) An automatic machine-implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

(1) determining a critical path length (C) of the layout portion;

(2) determining a minimum path length (MPL) for every path within the layout;

(3) unlocking all branches of the layout;

(4) determining any branches of the paths in the layout where the minimum path length (MPL) for that path is equal to the critical path length (C) and locking those branches of the layout;

(5) determining whether any branches of the layout remain unlocked, if no branches remain unlocked then the method is complete;

(6) determining which of the unlocked branches of the layout has the smallest actual spacing and designating that branch as the branch (K) for processing;

(7) determining the width of the spacing between the neighbor branches on either side of branch (K);

(8) determining whether the actual spacing of the branch (K) plus a predetermined incremental spacing is less than or equal to the larger of the spacing of that unlocked branch that is the predecessor branch and less than or equal to the spacing of the unlocked branch that is the successor branch, and if the spacing of the particular branch (K) plus the predetermined incremental spacing is not less than both the spacing of the predecessor branch and the spacing of the successor branch, locking the particular branch (K) and returning to the step (5);

(9) determining whether the graph connectivity restrictions of the layout allow the spacing of the particular branch (K) to be increased by the predetermined incremental spacing, if the graph connectivity restrictions of the layout does not allow the spacing for the particular

branch (K) to be increased, locking the particular branch and returning to the step (5);

(10) increasing the spacing of the particular branch (K) by the predetermined incremental spacing;

(11) updating the graph connectivity of the layout; and

(12) returning to step (5).

32. (New) The method of Claim 31, and further comprising:

(13) subsequent to performing step (10) and prior to performing step(11), decreasing the spacing of the larger of the predecessor branch and the successor branch to the branch (K) by the predetermined incremental spacing.

33. (New) The method of Claim 31, wherein the critical path length (C) represents a dimensional constraining below which the layout portion cannot be reduced in size in a particular direction.

34. (New) The method of Claim 31, wherein the minimum path length (MPL) represents the smallest path length in which the features and the spacing of a particular path can be disposed while still preserving connectivity to other paths in the layout.

35. (New) A machine-readable medium having recorded on it a set of instructions for performing an automatic machine-implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

(1) determining a critical path length (C) of the layout portion;

(2) determining a minimum path length (MPL) for every path within the layout;

(3) unlocking all branches of the layout;

(4) determining any branches of the paths in the layout where the minimum path length (MPL) for that path is equal to the critical path length (C) and locking those branches of the layout;

(5) determining whether any branches of the layout remain unlocked, if no paths remain unlocked then the method is complete;

(6) determining which of the unlocked branches of the layout has the smallest actual spacing and designating that branch as the branch (K) for processing;

(7) determining the width of the spacing between the neighbor branches on either side of branch (K);

(8) determining whether the actual spacing of the branch (K) plus a predetermined incremental spacing is less than or equal to the larger of the spacing of the unlocked branch that is the predecessor branch and to the spacing of the unlocked path that is the successor branch, and if the spacing of the particular branch (K) plus the predetermined incremental spacing is not less than both the spacing of the predecessor branch and the spacing of the successor branch, locking the particular branch (K) and returning to the step (5);

(9) determining whether the graph connectivity restrictions of the layout allow the spacing of the particular branch (K) to be increased by the predetermined incremental spacing, if

the graph connectivity restrictions of the layout does not allow the spacing for the particular branch (K) to be increased, locking the particular branch (K) and returning to the step (5);

(10) increasing the spacing of the particular branch (K) by the predetermined incremental spacing;

(11) updating the graph connectivity of the layout; and

(12) returning to step (5).

36. (New) The machine readable medium of Claim 35, and further comprising:

(13 ) subsequent to performing step (10) and prior to performing step(11), decreasing the spacing of the larger of the predecessor branch and the successor branch to the branch (K) by the predetermined incremental spacing.

37. (New) The machine readable medium of Claim 35, wherein the critical path length (C) represents a dimensional constraining below which the layout portion cannot be reduced in size in a particular direction.

38. (New) The machine-readable medium of Claim 35, wherein the minimum path length (MPL) represents the smallest path length in which the features and the spacing of a particular path can be disposed while still preserving connectivity to other paths in the layout.

39. (New) A system operable to dc-compact a layout for a portion of an integrated circuit, said system comprising a processor specially adapted to perform an automatic machine implemented method of de-compacting a layout of a portion of an integrated circuit, comprising:

(1) determining a critical path length (C) of the layout portion;

(2) determining a minimum path length (MPL) for every path within the layout portion;

(3) unlocking all branches of the layout portion;

(4) determining any branches of the paths in the layout portion where the minimum path length (MPL) for that path is equal to the critical path length (C), and locking those branches of the layout;

(5) determining whether any branches of the layout remain unlocked, if no branches remain unlocked then the method is complete;

(6) determining which of the unlocked branches of the layout has the smallest actual spacing and designating that branch as the branch (K) for processing;

(7) determining the width of the spacing between the neighbor branches on either side of branch (K);

(8) determining whether the actual spacing of the branch (K) plus a predetermined incremental spacing is less than or equal to the larger of the spacing of that unlocked branch that is the predecessor branch and less than or equal to the spacing of the unlocked branch that is the successor branch, and if the spacing of the particular branch (K) plus the predetermined incremental spacing is not less than both the spacing of the predecessor branch and the spacing of the successor branch, locking the particular branch (K) and returning to the step (5);

(9) determining whether the graph connectivity restrictions of the layout allow the spacing of the particular branch (K) to be increased by the predetermined incremental spacing, if

the graph connectivity restrictions of the layout does not allow the spacing for the particular branch (K) to be increased by the predetermined incremental spacing, locking the particular branch (K) and returning to step (5);

(10) increasing the spacing of the particular branch (K) by the predetermined incremental spacing;

(11) updating the graph connectivity of the layout; and

(12) returning to step (5).

40. (New) The system of Claim 39, and further comprising:

(13 ) subsequent to performing step (10) and prior to performing step(11), decreasing the spacing of the larger of the predecessor branch and the successor branch to the branch (K) by the predetermined incremental spacing.

41. (New) The system of Claim 39, wherein the critical path length (C) represents a dimensional constraining below which the layout portion cannot be reduced in size in a particular direction.

42. (New) The system of Claim 39, wherein the minimum path length (MPL) represents the smallest path length in which the features and the spacing of a particular path can be disposed while still preserving connectivity to other paths in the layout.